PVP 14

Code: EC3T6, EE3T6

II B.Tech - I Semester–Regular/Supplementary Examinations – November 2017

SWITCHING THEORY AND LOGIC DESIGN

(Common for EEE, ECE)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1. a) Convert the decimal number 250.5 to base 2.
   b) Write De-Morgan laws.
   c) Implement two input EX-OR gate from 2 to 1 multiplexer.
   d) Write the demerits of PROM.
   e) What is race around condition?
   f) Write the difference between Mealy and Moore machine.
   g) Show that $A \oplus B \oplus (A + B) = \bar{A}B$
   h) Simplify the Boolean Expression $AB + \bar{A}C + B\bar{C} + \bar{B}D + \bar{D}$E
   i) Convert SR Flip Flop to D-Flip Flop.
   j) Write differences between combinational and Sequential Logic Circuits.
   k) Draw the logic circuit for 4-bit Ring Counter.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. Decode the message assuming that at most a single bit error occurred in each code word when it is transmitted through a noisy channel using 7-bit Hamming code.
   1110111, 0011011, 1101101, 1011101 16 M

3. Using K-Map obtain minmal SOP for the given function.
   $f(ABCDE) = \sum 18,19,20,21,22,23,26,29,30,31 + d\,(10,11,13,14,15,27,28)$
   and draw the logic circuit for simplified expression using only NAND gates. 16 M

4. a) Realize the following functions using Decoders and additional OR gates. 8 M
   (i) $F_1 = AB + \bar{B}C + A\bar{D}$
   (ii) $F_2 = \sum(0,1,3,5,13,14,15)$
   (iii) $F_3 = \prod(0,1,3,10,14,15)$

   b) Realize the following function using 8 to 1 multiplexer.
   $F(A,B,C,D) = \sum(0,1,3,5,9,11,13,15)$ 8 M

5. a) Design a modulo-12 up synchronous counter using T- flip flops and draw the circuit diagram. 8 M

   b) Explain synchronous and ripple counters. Compare their merits and demerits. 8 M

6. a) Give the block diagram of synchronous and asynchronous sequential circuits and list out the merits and demerits. 8 M

b) Design clocked sequential circuit with single input and single output to produce an output Z= 1 when ever the input X completes sequence of pulses 10101 overlapping is also allowed. Draw the circuit using T-Flip Flop. 8 M